REMARKS

Reconsideration and allowance are requested.

Claims 1-22 stand rejected under 35 U.S.C. §101. In a telephone conference on December 6, 2007, the Examiner informed the undersigned that this rejection was withdrawn.

Claims 1-22 stand rejected under 35 U.S.C. §102 for anticipation based on Chen. This rejection is respectfully traversed.

The claims relate to performing more quickly an absolute difference calculation on portions of first and second data elements in a data processing apparatus. Quicker calculation is particularly advantageous in the light of the ever shorter clock cycles being implemented in contemporary data processing apparatuses.

Chen describes a floating-point calculation apparatus. A difference between exponent values and an inverted value thereof is calculated using a subtractor. One of the difference and the inverted difference values is selected in accordance with a signal indicating which of the exponent values is greater. Because only one subtractor is used, reduced circuit scale, chip real estate, and power consumption can be achieved.

During telephone discussions with the Examiner, it was explained that in the context of the combination of features recited in independent claims 1 and 12, Chen failed to disclose or suggest the following quoted from claim 1: "wherein the adder circuitry is configured to invert the portion of the second data element, and wherein comparison circuitry is configured to set the comparison result as input to the adder circuitry to a logical 0 value if the second data element is the larger data element and to a logical 1 value otherwise." A similar feature in method format is recited in claim 12.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

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